CLAIMS

1. A method to adjust an operating parameter of a magnetoresistive random access memory having a tunable circuit comprising:

measuring the operating parameter of the magnetoresistive random access memory to obtain a measured operating parameter result;

tuning the tunable circuit based on the measured operating parameter result.

2. The method of claim 1 with tuning the tunable circuit comprising tuning by tuning a bias control circuit.

3. The method of claim 1 with measuring the operating parameter comprising measuring the operating parameter in the form of a word reference current.

4. The method of claim 1 with measuring the operating parameter comprising measuring the operating parameter in the form of a sense reference current.

5. A method to adjust an operating parameter of a plurality of magnetic random access memories each having a tunable circuit comprising:

measuring the operating parameter of at least one of the magnetic random access memories to obtain a measured operating parameter result; and

tuning at least one of the plurality of the tunable circuits based on the measured operating parameter result.

6. The method of claim 5 with tuning at least one of plurality of the tunable circuits comprising tuning at least one of the plurality of the tunable circuits by tuning a bias control circuit.

7. The method of claim 5 with measuring the plurality of magnetic random access memories constructed on a single wafer.

8. The method of claim 5 with measuring the operating parameter comprising measuring the operating parameter in the form of a word reference current.

9. The method of claim 5 with measuring the operating parameter comprising measuring the operating parameter in the form of a sense reference current.

10. A bias tuning circuit for a MRAM comprising, in combination:

a bias generator having a bias output;

a plurality of switches having a word reference input and a mirror transistor output;

a plurality of mirror transistors connected to one of the mirror transistor outputs;

a transistor connected in a mirror configuration with the plurality of mirror transistors having a tuned reference output; and

a selector to select one of the mirror transistor to activate the transistor to set the voltage to the plurality of mirror transistors.

11. The bias tuning circuit of claim 10 with the each one of the plurality of mirror transistors having a different gain.

12. The bias tuning circuit of claim 10 further comprising, in combination:

a pad;

a indicator transistor in a mirror configuration with the transistor connected to the pad to provide an indicator.

13. The bias tuning circuit of claim 12 with the pad being an external pad.

14. The bias tuning circuit of claim 12 with the indicator transistor having a gain that is a multiple of the transistor.

15. The bias tuning circuit of claim 10 with the plurality of mirror transistors are n-channel transistors.

16. The bias tuning circuit of claim 10 with the plurality of switches being transistors.

17. The bias tuning circuit of claim 10 with the transistor being an N-channel transistor.

18. The bias tuning circuit of claim 10 with the bias generator being a temperature and voltage compensated bias generator.

19. The bias turning circuit of claim 10 with the selector selecting one of the plurality of mirror transistors to compenstate of a tested parameter.

20. The bias tuning circuit of claim 10 with the tested parameter being manufacturing variance.